REMARKS

Claims 1-46 are pending in the present application. Claims 1, 4, 5, 13, 16, 17, and 27 have been amended. Claims 36-46 are new. Claims 1-3, 13-15, 28, and 32 are independent.

OBJECTIONS TO THE SPECIFICATION

In the Office Action, the Examiner has objected to the specification because the characters "n and N" on page 3, lines 5 and 7, are allegedly ambiguous. Applicant respectfully submits that these symbols are not ambiguous because they are clearly defined in the specification. Page 1, line 17, defines the symbol "N" as the dividend; while page 3, lines 6-8, disclose that the symbol "n" represents the number of bits of which the divisor D is comprised. Accordingly, Applicant respectfully submits there is no ambiguity between these symbols.

The Examiner has also objected to the specification because equations 5 and 7 of page 5 each define N as having two different value ranges. Applicant respectfully disagrees with the Examiner's assessment. Specifically, the different formulas for N defined in equation 5 **are equivalent**.[1] Equations 10-12 show that the quotient and remainder for D+1 are made up of the high n bits and low n bits, respectively, of N. Therefore, the purpose of equations 5 and 7 is to

[1] This can be shown by expanding each formula:
$Q*(D+1)+(R-Q) = Q*D+Q+R-Q = Q*D+R$;
$(Q-1)*(D+1)+[(R-Q)+(D+1)] = Q*D-D+Q-1+R-Q+D+1 = Q*D+R$.

transform the equation N = Q * D + R into the form N = Q' * (D+1) + R', where R' > 0.[2] Equation 9 shows the relationship between the remainder and the terms Q' and R'. Therefore, by determining Q' and R' as the high and low n bits of N, respectively, and then applying Equation 9, the remainder can be determined without applying an iterative algorithm.

In view of the above explanation, Applicant respectfully submits that equations 5 and 7 are not in error. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the objections to the specification.

35 U.S.C. § 112, FIRST PARAGRAPH, REJECTION

Claims 1-35 stand rejected under 35 U.S.C. § 112, first paragraph, for failing to disclose the procedure "to force Divisor to always stay equal 2^n-1 or alternative means to implement should it impossible to fix the value of N to make the system operational." (section 3.1 of the Office Action).

35 U.S.C. § 112, first paragraph, requires that the specification describe how to make and use the claimed invention. Accordingly, Applicant assumes that the Examiner has rejected these claims under § 112, first paragraph, because he believes that the specification is not enabling for determining whether the values of D and N meet the

[2] Since R' > 0, we must define R' and Q' differently for the case where R ≥ Q and the case where R < Q.

conditions of $D = 2^n-1$ and $0 < N < (2^n-1)^2$. Applicant respectfully disagrees.

The test for determining whether the features of a claim are enabled by the specification, for purposes of § 112, first paragraph, is to determine whether one of ordinary skill in the art could only make or use the claimed invention with undue experimentation. See MPEP § 2164.01. Applicant respectfully submits that one of ordinary skill would be able to implement the claimed conditions for D and N without undue experimentation. For example, one of ordinary skill would know how to implement Conditions 1 and 2 shown on page 7, lines 3 and 4, either as computer program instructions or using hardware logic elements. Further, the specification discloses on page 3, lines 22-28, that the present invention may be used in connection with an application where such conditions are already satisfied, such as Reed-Solomon coding.

In section 3.1 of the Office Action, the Examiner states, "It is apparent that if there is no doubt as to the value of the divisor, no computation recursive or iterative or otherwise for a remainder is required." Applicant is perplexed by this statement. To process any N mod D operation, the value of the divisor D **must** be known. The only way that a computation of a remainder can made is when the dividend N and divisor D are known. Accordingly, it is unclear what the Examiner's rationale is for stating that no calculation is required when the divisor is known.

Applicant respectfully submits that the present specification and claims meet the requirements of § 112, first paragraph. Should the Examiner choose to maintain this rejection, Applicant respectfully requests the Examiner to more clearly explain why the claims are not enabled. Reconsideration and withdrawal of this rejection is respectfully requested.

35 U.S.C. § 103(a) REJECTION – APPLICANT'S ADMITTED PRIOR ART

Claims 1-35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' Admitted Prior Art (hereafter AAPA). This rejection, insofar as it pertains to the presently pending claims, is respectfully traversed.

In the Office Action, the Examiner asserts that the AAPA, as described in page 1, line 7, to page 3, line 9, of the specification, teaches a computer-implemented procedure for performing modulo division, using a dividend N and an n-bit divisor D to produce a remainder R. The Examiner admits that AAPA fails to disclose non-iteratively processing N mod D, where $D = 2^n-1$ and $0 < N < (2^n-1)^2$.

The Examiner asserts that the technique of non-recursively processing a division operation to find a remainder is well-known. Particularly, the Examiner alleges that, when the divisor is 2, one can easily determine whether the remainder is one or zero based on the last

bit of the dividend. The Examiner alleges that it would have been obvious to modify the AAPA procedure by restricting divisor and dividend values to a suitable range, in view of the Examiner's example, because "such modification would provide the procedure disclosed in [AAPA] with a technique wherein computation of remainders can be effected by simple inspection of the dividend digits." (second full paragraph in page 9 of the Office Action).

Applicant respectfully submits that the Examiner merely shows a method of non-iteratively processing N mod D which can only be used in the **singular case where D = 2**. The Examiner's proposed modification of AAPA does not anticipate the claimed invention because D = 2 **never** satisfies the condition of $D = 2^n-1$. This is true because D must comprise a whole number of bits (i.e., n must be an integer), and there is no integer value of n for which both conditions D = 2 and $D = 2^n-1$ are true.

Applicants respectfully submit that each independent claim recites the non-iterative processing of N mod D under the condition where $D = 2^n-1$. As discussed in MPEP § 2142, all of the claim limitations must be taught or suggested by the prior art to establish a *prima facie* case of obviousness. The Examiner's proposed modification of AAPA fails to teach or suggest that non-iterative processing of N mod D where $D = 2^n-1$, and therefore, fails to teach all of the claim limitations. Therefore, the Examiner has failed to establish *prima facie* obviousness.

Applicant respectfully requests the Examiner to reconsider and withdraw this rejection for the reasons set forth above.

35 U.S.C. § 103 REJECTION - AAPA/ORTON ET AL.

Claims 1-3, 7-14, 19-24, 28, 32, 34, and 35 stand rejected under 35 § U.S.C. § 103(a) as being unpatentable over AAPA in view of Orton et al., "New Fault Tolerant Techniques for Residue Number Systems," IEEE Transactions on Computers, Vol. 41, No. 11, Nov. 1992, pp. 1453-64 (hereafter Orton). This rejection, insofar as it pertains to the presently pending claims, is respectfully traversed for the following reasons.

In section 2.2, page 4, of the Office Action, the Examiner asserts that Orton describes an algorithmic approach to finding a remainder. Applicant respectfully disagrees. Orton discloses a system for representing a number in a residue number system (RNS). Such representation is used to simplify addition, subtraction, and multiplication operations by taking advantage of the fact that:

a (mod N) + b (mod N) = [a + b] (mod N);
a (mod N) – b (mod N) = [a - b] (mod N); and
a (mod N) * b (mod N) = [a * b] (mod N).

In RNS, each number is converted into residue form by evaluating its mod function with respect to one of a set of moduli (divisors) being used. Since Orton discloses the conversion of numbers into residue form, Orton inherently requires the calculation of the remainders for modulo division. However, contrary to the Examiner's assertion,

Applicant respectfully submits that Orton fails to disclose any particular method for calculating the remainder. Instead, Orton is primarily concerned with detecting errors made during calculations (see Abstract of Orton). The portion of Orton cited by the Examiner (first paragraph on page 1463) merely discusses the fact that errors can be reduced by changing the set of moduli, or divisors, being used.

Since, Orton does not disclose any type of method for non-iteratively processing N mod D, Applicant respectfully submits that Orton fails to remedy the aforementioned deficiencies of AAPA with respect to claims 1-3, 7-14, 19-24, 28, 32, 34, and 35. Accordingly, Applicant respectfully submits that these claims are not obvious over AAPA in view of Orton. Reconsideration and withdrawal of this rejection is respectfully requested.

35 U.S.C. § 103(a) REJECTION – AAPA/STOUT

Claims 1-3, 7-14, 19-24, 28, 32, 34, and 35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Stout, Basic Electrical Measurements, 2d Ed., 1960, pp. 82-85 (hereafter Stout). This rejection, insofar as it pertains to the presently pending claims, is respectfully traversed for the following reasons.

In section 2.3, page 6, of the Office Action, the Examiner alleges that Stout describes techniques for calculating a remainder. In

particular, the Examiner points to page 83 of Stout for disclosing "means to estimate or approximate mathematical results such as remainders."

Applicant respectfully submits that page 83 of stout discloses technique for using a slide rule to perform division calculations more accurately and precisely. Specifically, Stout discloses that the slide rule can be used to compute only the *difference from unity*. The difference from unity is not the same as the remainder. In other words, the difference from unity is determined by subtracting the divisor from the dividend (N – D). Conversely, a remainder is determined by subtracting the product of the quotient and the divisor from the dividend (N – Q*D).

Applicant respectfully submits that Stout fails to disclose anything with respect to calculating the remainder of a division calculation. Instead, Stout is concerned more with carrying out the division as precisely, i.e., to as many decimal points, as possible. Furthermore, Stout discloses nothing with respect to the conditions that the divisor D = 2^n-1.

Accordingly, Stout fails to remedy the deficiencies of AAPA with respect to claims 1-3, 7-14, 19-24, 28, 32, 34, and 35, as discussed above. Therefore, Applicant respectfully submits that these claims are not obvious over AAPA in view of Stout. Reconsideration and withdrawal of this rejection is respectfully requested.

35 U.S.C. § 103(a) REJECTION – AAPA/SAHA ET AL.

Claims 1-3, 7-14, 19-24, 28, 32, 34, and 35 stand rejected as being unpatentable over 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Saha et al., "Design and FPGA Implementation of Efficient Integer Arithmetic Algorithms," IEEE, April 4-7, 1993, pp. 4-7 (hereafter Saha). This rejection, insofar as it pertains to the presently pending claims, is respectfully traversed for the following reasons.

In section 2.4, pages 7-8, of the Office Action, the Examiner asserts that Saha discloses an algorithm for calculating a remainder, where "predetermined and constant values in division process enable simplicity of hardware implementation."

Applicant respectfully submits that Saha discloses an algorithm for calculating a mod b, which can be implemented in the hardware circuit disclosed in Fig. 5. However, Saha's disclosed algorithm requires that the reciprocal of b be pre-computed and remain constant (see Saha, page 4, section entitled "Algorithm"). Saha further discloses that the calculation of the reciprocal of a number (i.e., the reciprocal of b) requires O (log N) steps, where N is the number of bits in b (see Saha, page 2, first paragraph of section entitled "The Division Module using Chinese Remaindering Algorithm").

Applicant respectfully submits that Saha's calculations are therefore dependent on the number of bits of the divisor. Therefore, Saha teaches away from independent claims 2 and 14, which require

that the number of processing operations necessary is **independent** of the number of bits n in the divisor D.

Also, neither AAPA nor Saha teaches the condition that the divisor $D = 2^n-1$ (where n = the number of bits of the divisor), as required by independent claims 1 and 13. Further, none of AAPA and Saha discloses the summing of bits in the bits of the dividend N to obtain the remainder, as required by independent claims 3, 28, and 32.

Applicant respectfully submits that the Examiner has failed to show that the cited prior art teaches all of the features recited in independent claims 1-3, 13, 14, 28 and 32. Accordingly, Applicant submits that the Examiner has failed to establish a *prima facie* case of obviousness in connection with these claims, or the claims depending thereon. Reconsideration and withdrawal of this rejection is respectfully requested.

CONCLUSION

In view of the above amendments and remarks, reconsideration of the various rejections and allowance of claims 1-46 is respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number of (703) 390-3030, to conduct an interview in an effort to expedite prosecution in connection with the present application.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 12-2325 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY & PIERCE, P.L.C.

By: _____

John A. Castellano
Reg. No. 35,094
12355 Sunrise Valley Drive, Suite 350
Reston, Virginia 20191

JAC/JWR:kmh

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 1, 4, 5, 13, 16, 17, and 27 have been amended as follows:

1. (Amended) A computer-implementable method of performing modulo division, using a dividend N and an n-bit divisor D to produce a remainder R, said method comprising:

[when $D=2^n-1$ and $0\leq N\leq(D-1)^2$,] non-iteratively processing N mod D to produce the remainder R, where $D=2^n-1$ and $0<N<(D-1)^2$.

4. (Amended) The computer-implementable method of claim [1] 37, further comprising the step of subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

5. (Amended) The computer-implementable method of claim [2] 39, further comprising the step of subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

16. (Amended) The apparatus of claim [13] 41, said apparatus subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

17. (Amended) The apparatus of claim [14] 42, said apparatus subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

27. (Amended) The apparatus of claim [16] 13, wherein said apparatus is a component of a Reed-Solomon coder.

Claims 36-46 have been added.